STUDY OF SEMICONDUCTOR HETEROJUNCTIONS

OF ZnSe, GaAs and Ge

By A. G. Milnes and D. L. Feucht

February 1, 1971 - April 30, 1971

Prepared under Research Grant No.
NGR 39-087-002 by
CARNEGIE-MELLON UNIVERSITY
Electrical Engineering Department
Pittsburgh, Pennsylvania 15213

NASA Research Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Washington, D. C.

ABSTRACT

Single crystal layers of ZnS and ZnSe have been epitaxially grown on p-type GaP using an HCl close-spaced vapor transport system. Grown layer doping is accomplished using heavily doped source (ZnS, ZnSe) material and a zinc vapor diffusion process that reduces the number of compensating zinc vacancies. Experimental characteristics of nZnS-pGaP and nZnSe-pGaP diodes indicate dominance of the forward I-U relationship by space-charge-limited flow in the 10^3-10^4 ohm-cm ZnS and ZnSe. The reverse I-U characteristics of these devices agree qualitatively with a multistep tunneling process but show larger than expected reverse currents. The reverse bias capacitance is strongly frequency dependent in all devices studied. Forward injection electroluminescence was not observed from any of the nZnS-pGaP and nZnSe-pGaP devices studied.

Further studies were conducted in the iodine system to grow a thin pGe layer followed by a n-type Ge layer on nGaAs to produce a Ge-GaAs transistor. A method using diborane as a dopant was developed to grow the p-type Ge without a thin intermediate n-type Ge layer at the interface. Measurements of an n-Ge-n-GaAs heterojunction yielded a barrier height of 0.37 eV in the conduction band.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

I. INTRODUCTION

During this report period the grant entered the final phase of its step funding. The effort during this period was devoted to completing work on the growth of ZnS and ZnSe on GaP and to continuing the Ge-GaAs junction studies.

Work on ZnS and ZnSe on GaP was completed and a paper prepared for publication. This appears as section II of the report. This work resulted in the first nZnS-pGaP and nZnSe-pGaP junctions prepared but the I-U characteristics were shown to be dominated by space charge flow in the ZnSe and ZnS in the forward direction and tunneling in the reverse.

A procedure was developed using diborane as a dopant for growing pGe on nGaAs without the introduction of an intermediate n layer in the Ge at the interface. This should enable the subsequent fabrication of a nGaAs-pGe-nGe transistor during the next period.

II. THE GROWTH AND ELECTRICAL CHARACTERISTICS OF EPITAXIAL LAYERS OF ZnS AND OF ZnSe ON p TYPE GaP

1. INTRODUCTION

Over the past decade there has been an ever increasing interest in the properties and the device feasibility of III-V and II-VI compound semiconductors. The wide band gaps and high mobilities of some III-V and II-VI compounds make them attractive for use in high operating temperature devices, in semiconductor lasers and light-emitting devices and in certain high-frequency applications. However, the technology of III-V and II-VI compounds is somewhat behind that of Ge and Si (especially in regards to crystal perfection). Most of the II-VI compounds have the added disadvantage of being not easily doped p and n type and are very easily self-compensated. Crystals that are combinations of III-V and II-VI compounds have been synthesized in the hope of obtaining the favorable wide band gap properties of a II-VI with the favorable doping properties of a III-V, but with limited success. Heterojunctions between II-VI and III-V semiconductors offer an alternative approach to combining the favorable properties of the II-VI and III-V compound semiconductors.

The initial interest in semiconductor heterojunctions was centered about improving the injection efficiency of transistors using a wide band-gap emitter-narrow band-gap base heterojunction [1]. Such "heterojunction" transistors have been fabricated using heterojunctions of CdS/Si [2] [3], GaAs/Ge [4], ZnSe/Ge [5] and ZnSe/GaAs [6]. The current gain of these devices tends to be in the range 10-50 and appears to be limited by defect components of emitter current caused by interface states or defects near the interface. At present research on the heterojunction transistor is being continued along the lines of improving the heterojunction interface by investigating new heterojunction pairs and different methods of heterojunction fabrication.

Recently, interest in heterojunctions has been stimulated by the excellent performance of double confinement mode lasers using heterojunctions of $Al_xGa_{1-x}As$-GaAs [7] [8]. Also forward bias junction electroluminescence has been

observed in several heterojunctions, CdS/ZnTe [9], ZnSe/ZnTe [10] [11], GaP/GaAs [12], ZnSe/GaP [13], ZnTe/CdSe [14].

The choice of semiconductors to be used in heterojunctions is primarily governed by the need to avoid mismatch or mechanical stress at the interface which might introduce defect states in the band gap of either semiconductor. Such defect states severely limit the performance of most semiconductor heterojunction devices.

In this study the heterojunction pair ZnS-GaP was chosen for investigation since (1) the lattice match is close and strain at the interface was not expected to be overly great and (2) the expected band diagrams from electron affinity considerations are favorable for forward bias injection of minority carriers. This suggests that nZnSe-pGaP junctions may be promising for both transistor and electro-optical action. The lattice mismatch between cubic ZnS and GaP is about 1%. The thermal coefficient of expansion for the two materials differ by no more than 20% in the temperature range $30^{o}C$-$600^{o}C$. Other investigators have successfully grown ZnS on GaP [15] and on Si [16].

Some studies were also made of the ZnSe/GaP heterojunction pair although the lattice mismatch of 4% for these materials was expected to result in high densities of interface states.

2. EXPERIMENTAL

2.1 Heterojunction Preparation

ZnS and ZnSe were epitaxially grown upon GaP using the HCl close-spaced system described by Hovel and Milnes [17]. GaP, p-type, substrates were chemically polished in $2HNO_3$; HCl prior to growth. The resulting (111)B surface (terminating in phosphorous atoms) was mirror smooth while the opposite surface, (111)A, had a slightly rippled surface. A search of the literature suggests that at present no chemical etch has been discovered that will impart

a smooth surface to the (III)A face of GaP. All growths of ZnS, ZnSe were therefore made on the (III)B face of the GaP.

Immediately after the final chemical etch, GaP substrates were coated with a 2000 Å layer of SiO_2 grown by the oxidation of tetraethylortho-silicate (TEOS) at 430°C in a system designed after that described by Heunisch[18]. The SiO_2 layer was found necessary to prevent substrate etching during the growth process.

Large grain size ZnS and ZnSe were used as source material. Sources were lapped flat to 3μm and degreased. Before growth the ZnS was etched in concentrated H_3PO_4 and the ZnSe was etched in concentrated HCl. All growth runs were made with the HCl system parameters given below:

T_{source}	780°C
T_{seed}	650°C
[HCl] in H_2	0.04%
Total Gas Flow Rate	200cc/min
Source-Seed Spacing	12 mils
Cooling Rate	1°C/min

Growths were cooled slowly to minimize ZnS and ZnSe cracking due to lattice and thermal expansion differences.

N-type doping of grown ZnS and ZnSe layers was achieved by using Al doped ZnS and Ga doped ZnSe sources, coupled with a processing step involving a zinc overpressure to suppress zinc vacancies.

The ZnS was received doped to 100 ppm Al. The ZnSe was undoped as received and had to be doped with Ga using the liquid zinc alloy process described by Aven [19]. The electron concentration in the al doped ZnS was $5x10^{16} cm^{-3}$ and in the Ga doped ZnSe was $1x10^{17} cm^{-3}$. A zinc overpressure scheme to suppress donor-compensating zinc vacancy acceptors that formed in the grown ZnS, ZnSe layers at the elevated growth temperature was achieved by sweeping zinc vapor over the grown layers as they cooled slowly after growth [17].

2.2 Electrical Measurements

N-type ZnSe and ZnS layers 4μm thick were grown on (111)B oriented p-type GaP slices cut from the same boule. Growth chips were diced and 1-2μm of ZnSe or ZnS was chemically removed with 2% bromine in methanol and hot concentrated phosphoric acid (90°C), respectively. This etching step was necessary to remove any compensated surface layers. In the case of ZnS the phosphoric acid treatment also promoted wetting of In contacts. Next, mesas were etched with $HCl:HNO_3$ to reduce surface leakage currents and to define cross-sectional areas for current flow. The p-type GaP was alloyed to a header and contacted at 450°C using a Ga-25% Zn alloy. Contact to the n-type ZnSe and ZnS was made (with the chip on a header) using an In dot or an In-Hg amalgam alloyed at 350°C. All contact processes used 2-5% HCl gas in Ar-15% H_2 as a flux [20].

The contacts to the ZnSe, ZnS and GaP were not perfectly ohmic above $100A/cm^2$ at 300°K. At 77°K contact quality was further degraded by increased contact resistance and increased GaP resistivity due to partial freeze-out of the 0.064 eV Zn level in GaP [21]. Better GaP ohmic contacts might be achieved if the alloying temperatures could exceed 450°C. For instance Dierschke and Pearson [22] have produced contacts to p-type GaP with Au-5% Zn alloyed at 650°C for 5 minutes in an H_2 atmosphere. However in this work a temperature of 650°C must be ruled out since it would crack the grown ZnSe and ZnS layers due to the necessary rapid thermal cycling as well as driving the grown layers high in resistivity by the loss of Zn.

I-U characteristics were measured at 300°K by placing devices under vacuum, in N_2 gas ambient and in room air. At 77°K the I-U measurements were made with devices under vacuum and directly immersed in liquid nitrogen. At 300°K and 77°K no measureable difference in results was found between the different methods. A Fluke 825A differential voltmeter and a Keithley Instruments 600A electrometer were used to measure voltage and current, respectively. C-U measurements were

performed at 1 MHz using a General Radio Co. Type 821-A Twin-T bridge. At 1 KHz a General Radio Co. Type 1608-A Impedance Bridge was used.

3. RESULTS

3.1 Expitaxial Growth

Single crystal ZnS and ZnSe films were grown on (111)B oriented GaP. Growths were from 3-4μm thick. Laue x-ray back-reflection patterns of a 15μm ZnS growth on (111)B GaP revealed a six-fold rotational symmetry that corresponded to the ZnS. The ZnSe surface morphology was almost featureless and very smooth whereas the as-grown ZnS morphology showed a little more texture. The growth rates were 6μm/hr and 3μm/hr for ZnSe and ZnS, respectively, for the HCl system growth parameters given in section 2. No grown-layer cracks were observed as long as the cooling rate was less than 2^{o}C/min.

Both ZnSe and ZnS growths showed smooth unetched GaP surfaces after partial selective ZnSe and ZnS removal in concentrated HCl. The morphology of the grown ZnS layer and an exposed GaP surface are shown in Fig. 1. The lines in the GaP region are probably interface misfit (slip) traces revealed by the HCl.

As-grown and beveled ZnS surfaces were treated in chromic acid to reveal defect structure and interfacial solid-solution transition regions. No ZnS-GaP solid-solution was revealed, Fig. 2, although the ZnS-GaP system is reported to form mixed crystals in all proportions [23]. Fig. 3 shows slip lines and etch pits in the ZnS indicating that the ZnS (on GaP) is under considerable strain. The ZnS etch pit density is approximately 10^{8}cm^{-2} and is about two orders of magnitude larger than that of the GaP substrate (measured before and after growth and found to remain constant).

Typical grown ZnS and ZnSe n-type resistivities ranged from 10^{6}-10^{8}ohm-cm if a ZnS overpressure was not present as the growth cooled. Zinc vapor pressures of 50-100 mHg in the vicinity of the cooling grown layers reduced the ZnS, ZnSe resistivity to 10^{3}-10^{4} ohm-cm provided the ZnS, ZnSe sources were heavily

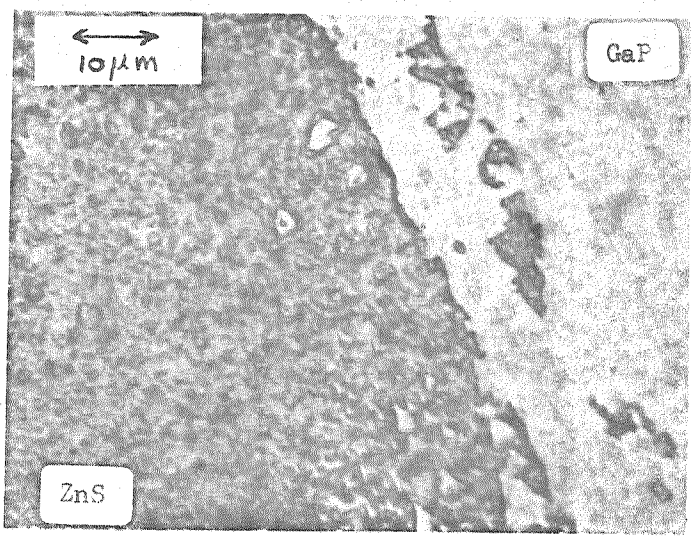

Fig. 1. ZnS-GaP interface with ZnS partially removed. (Specimen CS-66).

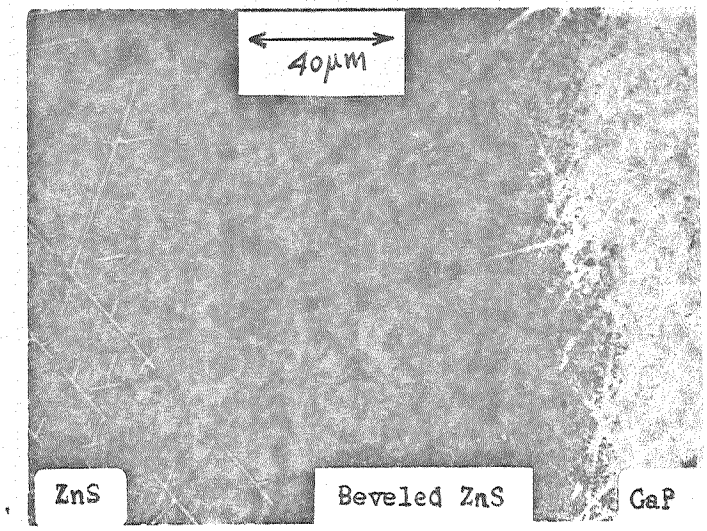

Fig. 2. Angle lapped ZnS-GaP interface treated with chromic acid. No apparent ZnS-GaP solid solution region is revealed. (Specimen CS-66).

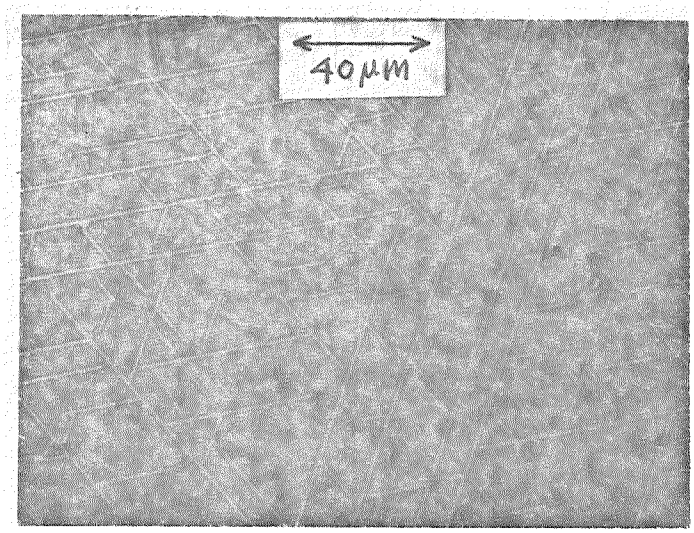

Fig. 3. As-grown ZnS surface etched in chromic acid. Slip lines and etch pits are revealed. (Specimen CS-66).

doped with Al and Ga, respectively. Undoped ZnS, ZnSe sources produced 10^6 ohm-cm grown layer resistivities after the zinc step.

3.2 Electrical Characteristics

A typical log I versus log U forward characteristic of an nZnS-pGaP diode is give in Fig. 4. This characteristic is relatively temperature insensitive with a high power law dependence at low biases followed by a break into a lower power law region. The high bulk resistivity of the ZnS makes it improbable that characteristics of the form

$$I = I_o \exp \frac{qU_a}{kT} \qquad (1)$$

associated with thermal injection over a barrier could be observed, even if eqn(1) should represent the actual junction voltage-current relationship. Instead the observed device voltage appears to be dominated by the space-charge limited flow component in the ZnS.

Fig. 5 shows a similar power law I-U relationship for an ZnSe-pGaP diode.

The reverse characteristic of an nZnS-pGaP diode plotted as log I versus log U is given in Fig. 6. This characteristic is also moderately temperature insensitive. A low power-law is observed at low biases with a break into a high power-law region at higher biases.

Practically all nZnS-pGaP devices had a large degree of noise and jitter associated with both the forward and reverse characteristic. The entire V-I characteristic shifted about (2-5 shifts/sec.) when viewed on an oscilloscope curve tracer and in most cases was unmeasurable by dc technique. Light from an incandecent lamp focused on nZnS-pGaP and nZnSe-pGaP diodes did not reduce the jitter or the noise. Usually the worst jitter was seen in the reverse direction and was an order of magnitude greater in magnitude on nZnSe-pGaP devices than in n-ZnS-GaP devices. Consequently, no measured reverse characteristic can be presented for nZnSe-pGaP devices. The forward characteristic of the nZnSe-pGaP diode shown in Fig. 5 was reasonably noise-free.

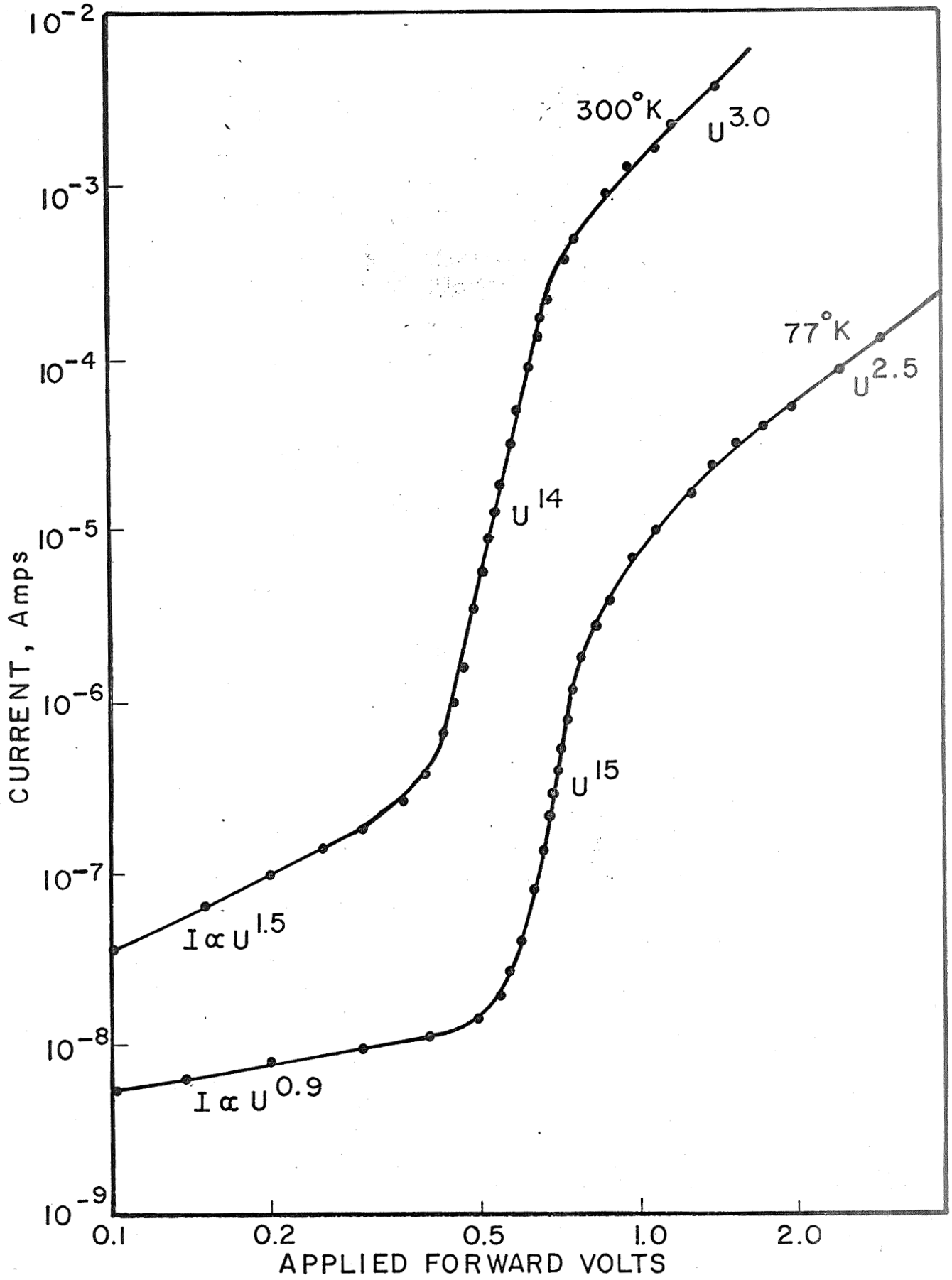

Fig. 4. nZnS-pGaP forward logU-logI characteristic. The high power law followed by a low power law suggest space-charge flow with traps. The ZnS resistivity is 5×10^{3} ohm cm. (Specimen CS-66A).

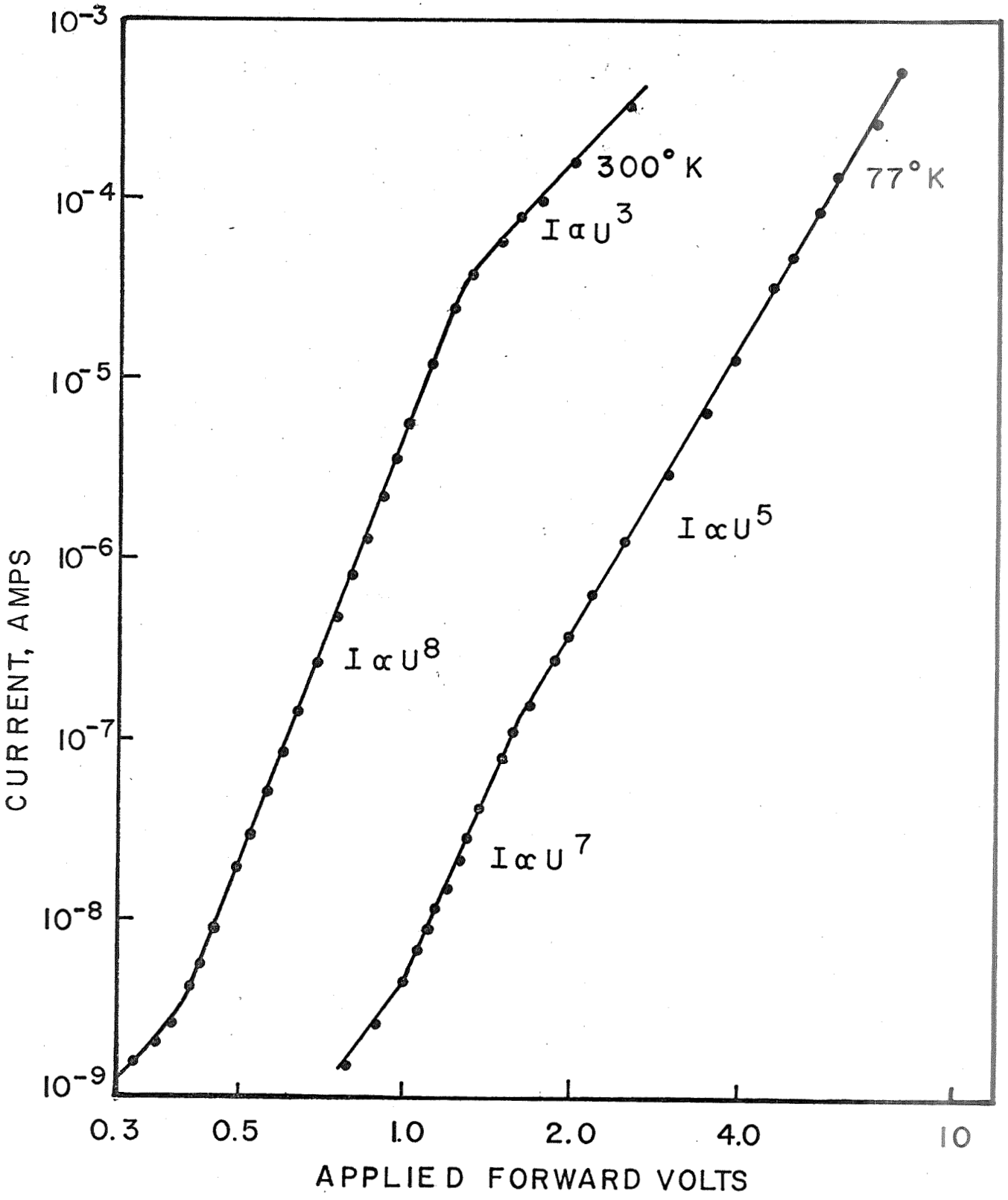

Fig. 5. nZnSe-pGaP forward logU-logI characteristic. The high power law suggests space-charge-limited flow with traps. The ZnSe resistivity is 5 x 10^3 ohm cm. (Specimen CS-67).

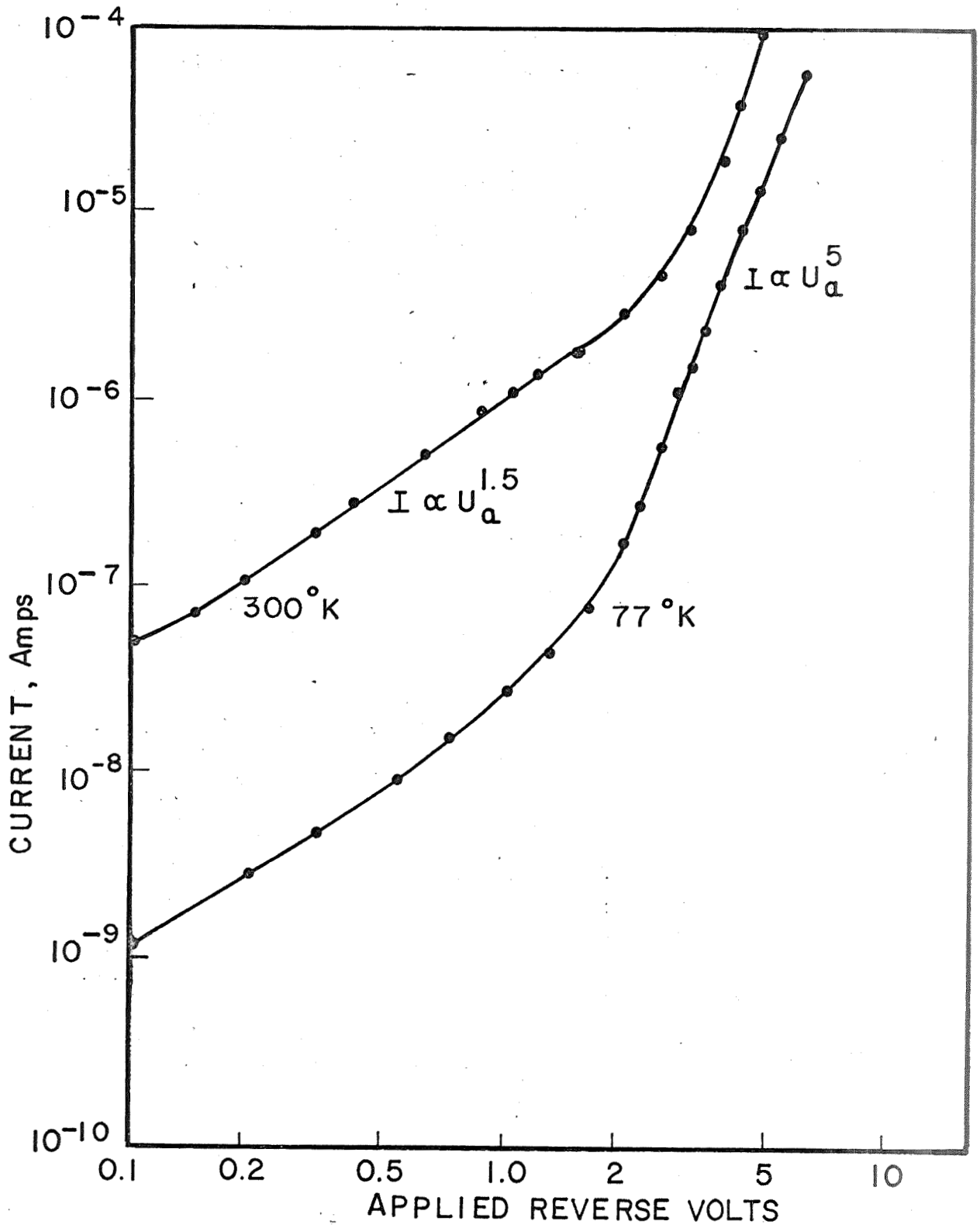

Fig. 6. Reverse logU-logI characteristic of an nZnS-pGaP diode. (Specimen CS-66A).

The noise and jitter was not due to contacts. Many devices had more than one contact per semiconductor, and the V-I relationship between two contacts on either the ZnS or the GaP was always linear and noise free at current densities up to 100 A/cm^2 (about 10 mA). No noise or jitter occurred above 100 A/cm^2, but the contacts began to deviate from linearity above this current density. Schottky barrier diodes of excellent rectification ratios were made with indium on material from the same GaP slice as used for the nZnS-pGaP devices and did not show any noise or jitter.

The capacitance reverse-voltage characteristic of an nZnS-pGaP diode is given in Fig. 7. The straight line "best fit" characteristics are of the form

$$C \propto (U_a + U_D)^{-r} \qquad (2)$$

where r was about .04 and C is the capacitance, U_a is the applied reverse voltage and U_D is a constant that is associated with the built-in heterojunction potential. Both C and U_D are frequency dependent. Capacitance reverse-voltage data for nZnSe-pGap devices were not obtainable due to excessive noise.

An attempt was made to observe optical radiation from forward biased nZnS-pGaP and nZnSe-pGap heterojunctions. Devices were mounted flush with the cathode face of a 7102 photomultiplier tube (S1 response) and pulsed to forward current densities as high as 2×10^3 Amp/cm^2. Pulse widths ranged from 2-10 μsec. Devices were examined at 300^oK.

No light was detected in the spectral range (0.3μm to 1.2μm) of the 7102 photomultiplier tube.

4. DISCUSSION OF THE RESULTS

4.1 Epitaxial Growth

The well defined Laue spot-patterns obtained from thick ZnS growths indicate that the growth is not polycrystalline. However the crystalline quality of the grown layers could not be determined from spot patterns. Crystal perfection is best determined by other x-ray methods (x-ray rocking curves and diffraction

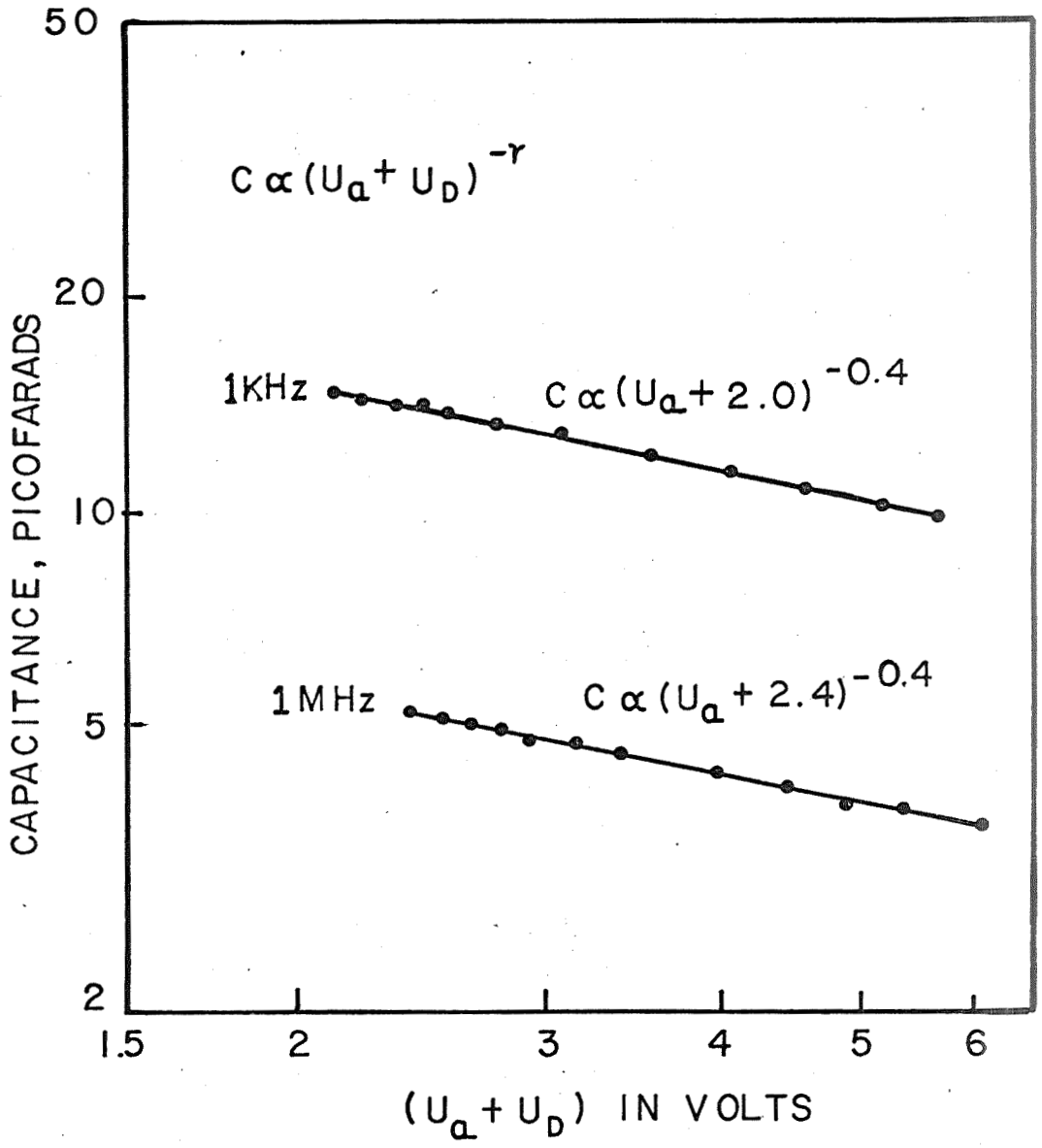

Fig. 7. Reverse bias capacitance characteristic of an nZnS-pGaP diode. (Specimen CS-66A, 300°K.)

contrast) not available for the present work. The six-fold symmetry observed in ZnS spot patterns may come either from a twinned (111) oriented structure or a (0001) oriented hexagonal or 6H polytype structure. Between the growth temperature and 300°K, both hexagonal and cubic forms of ZnS may exist. The cubic phase appears as a twinned structure with (111) planes parallel to the (0001) planes of the hexagonal phase. Bertoti et al. [15] observed that ZnS grown on (111)B GaP at 740°C-880°C had a hexagonal or 6H polytype structure. More x-ray analysis would be necessary to determine the structure of the ZnS grown in this study. One can only infer from the x-ray patterns that the ZnS overgrowth is oriented either (111) or (0001) which might be expected since the GaP is (111) oriented.

Bertoti et al [15] report a transition layer at the interface of ZnS-GaP grown in an HCl closed-tube vapor transport process using GaP substrate temperatures ranging from 740°C-880°C (much higher than the 650°C of this study). This layer is attributed to chemical attack of the GaP with subsequent formation of a ZnS-GaP solid solution at the interface. No such transition region was observed in this work (see Fig. 2). The low substrate temperatures and HCl concentrations used here have probably prevented significant chemical attack on the GaP.

The high density of etch pits revealed by the chromic acid etch indicates that the grown ZnS is imperfect even though regular well-defined Laue spot patterns are obtained. The defects could be a result of strain relief at the ZnS-GaP interface or stacking faults in hexagonal regions of the ZnS that introduce regions of cubic disorder [25].

The lower limit to ZnS, ZnSe grown layer resistivity appears to be about 10^3 ohm-cm when using doped source material and zinc overpressures applied below the growth temperature as a means of doping grown layers. This rather high resistivity is probably due to low source to seed dopant (Al, Ga) transport ratios rather than inefficiencies in the zinc overpressure treatment. Separate experiments with bulk doped (Al) ZnS, (Ga) ZnSe in the growth system have shown

the zinc overpressure treatment to be as effective as the liquid ZnS technique of Aven [19] in reducing the zinc vacancy concentration.

4.2 I-U Characteristics, Theory

The proposed equilibrium (no applied bias) energy band diagram for an nZnS-pGaP heterojunction is shown in Fig. 8 (a). The band diagram for an nZnSe-pGaP heterojunction is similar except that E_g(ZnSe) is 2.68eV, ΔE_C is o.21eV, ΔE_V is 0.22eV, and qU_D is 2.1eV. These band diagrams were derived from the electron affinity difference model proposed by Anderson [25] and must be regarded as tentative in the absence of direct determination. The valence band interface discontinuity ΔE_V is equal to the difference between the sum of the electron affinity and energy band gap of the two materials. The diffusion potential, U_D, is equal to the Fermi level difference between the two materials before they are brought together and mostly appears in the moderately high resistivity n-type material due to the large difference in doping densities between the n and p regions. The model assumes that there is no charge at the interface. The hump in the GaP near the interface is the effect of Zn which has diffused into the GaP from the ZnSe during the zinc overpressure step. This diffused region may extend from 0.1 to 2μm into the GaP, depending on the zinc processing time and temperature.

The electron affinities used to construct the ZnS/GaP and ZnSe/GaP band diagrams are 4.09eV for ZnSe [26], 3.9eV for ZnS [27] and 4.3eV for GaP. There appears to be no report on a direct measurement of the electron affinity of GaP. Weinstein et al []7] have proposed that ΔE_C is equal to 0.22eV for pGaAs-nGaP junctions. This implies (from the Anderson heterojunction model) a GaP electron affinity of 4.3eV. In studying nGaAs-pGaP junctions Alferov et al. [28] dispute the ΔE_C value (.22eV) proposed by Weinstein et al. [29] and suggest an electron affinity of 3.0eV for GaP based on Au-nGaP metal-semiconductor barrier heights reported by Cowley and Heffner [30]. Furthermore Alferov et al. [29] use 3.65eV for the GaAs electron affinity when interpreting the GaAs-GaP behavior, which

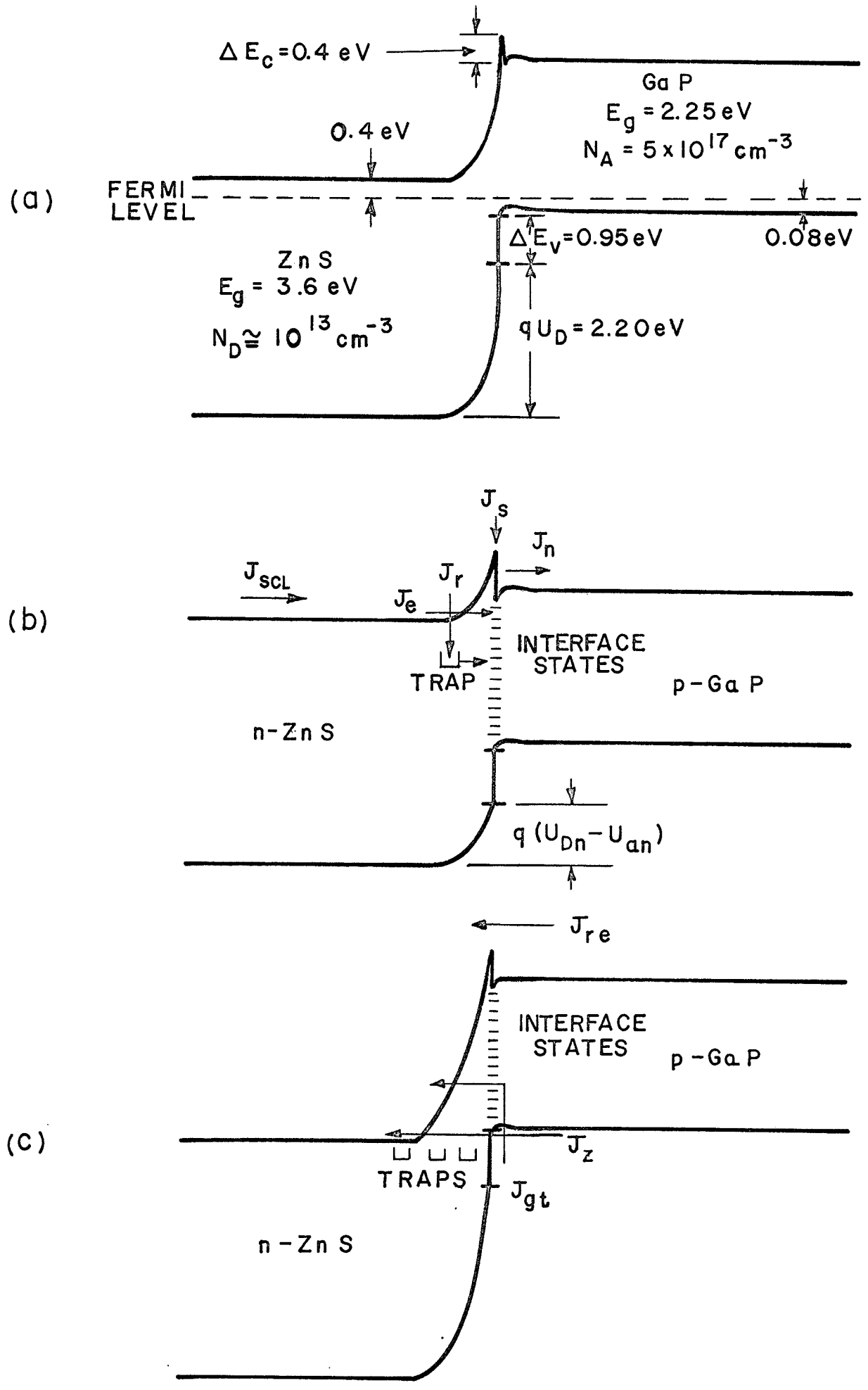

Fig. 8. Band diagrams of nZnS-pGaP heterojunctions;
A) Zero bias voltage.
B) Forward bias applied.
C) Reverse bias applied.

does not agree with the value 4.07eV reported by Gobeli and Allen [30]. Davis et al. [32] attempt to clarify the discrepancy in ΔE_C by examining n-n, p-n and n-p GaAs-GaP junctions. Their results suggest $0 < \Delta E_C < 0.1$ eV. In this study nZnS-pGaP capacitance data indicate a GaP electron affinity between 4.2 and 4.4 eV (using the Anderson model). Therefore an electron affinity value of 4.3 eV has been used for GaP in obtaining the diagram in Fig. 8(a).

Fig. 8(b) shows the proposed particle current densities at the interface under forward bias [n(-), p(+)]. Interface states and an unknown distribution of traps in the moderately high resistivity ZnS and ZnSe have been assumed. In the forward direction most of the applied voltage is across the high-resistivity n region resulting in the possibility of space-charge-limited current, J_{SCL}, in the bulk of the n region. Most of the voltage developed across the n and p region depletion regions is on the high resistivity n side and is designated $U_{Dn}-U_{an}$. The corresponding voltage across the p region depletion region is $U_{Dp}-U_{ap}$ [not labeled in Fig. 8(b)]. The diffusion voltage and total applied voltage are $U_D=U_{Dn} + U_{Dp}$ and $U_a = U_{an} + U_{ap}$, respectively.

First consider the particle current densities at the interface under forward bias. There are electrons tunneling directly from the n region conduction band into interface states to recombine with holes for a current density J_e; there are electrons recombining at the interface with holes for a current density J_s; there are electrons captured within the n region depletion width followed by tunneling to interface states (J_r) and there are electrons thermally injected into the p region conduction-band from the n region (J_n). There may also be additional recombination of n region electrons (not shown in Fig. 8(b) with p region holes that tunnel to n region traps or are injected into the n region and by generation-recombination processes. These latter processes have been neglected due to the moderately large value of ΔE_V and the large band gaps of ZnS and ZnSe.

The functional dependence of J_e, J_r, J_s and J_n has been developed by Hovel and Milnes [32]. They suggest that

$$J_e \propto \exp\left[-\alpha(U_{Dn}-U_{an})\right] \tag{3}$$

and

$$J_r \propto \exp\left[-\alpha(U_{Dn}-U_{an})\right] \tag{4}$$

for J_r limited by tunneling, where $\alpha = \frac{4}{3\hbar} R^{\frac{1}{2}} \left[\frac{m^* \varepsilon_n}{N_d}\right]$ (5)

also

$$J_r \propto N_D \exp\left[\frac{-q(U_{Dn}-U_{an})}{kT}\right] \tag{6}$$

where J_r is limited by electron capture by traps, and

$$J_s \propto N_d \exp\left[\frac{-q(U_{Dn}-U_{an})}{kT}\right] \tag{7}$$

where the interface recombination is limited by the n region electron supply, and

$$J_n \propto q\mu_n E_o N_D \exp\left[\frac{-(U_{Dn}-U_{an})}{kT}\right] \tag{8}$$

and

$$J_{SCL} = J_e + J_e + J_s + J_n \tag{9}$$

where μ_n is the injected electron mobility in the p region, E_o is the electric field at the interface (500-800 volt/cm) in the p region due to the diffused Zn impurity gradient, R is the number of tunneling steps (via traps), m* is the electron effecitve tunneling mass in the n region, ε_n is the dielectric coefficient of the n region, and N_D is the effective doping concentration in the bulk n-region.

Fig. 8(c) shows the reverse bias [n(+), p(-)] situation. The reverse current consists of J_{re} electrons in the p regions flowing over the hump and small barrier into the n region, J_Z due to Zener tunneling from the p region valence band to the n region conduction band either directly or via n-region traps, J_{gt} due to

electrons in the p region valence band being raised in energy to an interface state level followed by tunneling into the n region conduction band, and J_L, due to surface leakage. J_{gt} will be neglected since moderately large energies are necessary to raise valence band electrons to interface state levels. J_{re} quickly saturates when $U_{Dp}-U_{ap} > \Delta E_C$.

At high reverse bias the p region valence band may become level with the n region conduction band allowing Zener tunneling to occur. The current for this process has been described by Riben and Feucht [33] and is

$$J_Z \propto U_{an} \exp \left[\frac{-\alpha E^{1/2}}{R-1/2} (E_{gn} - \Delta E_V) \ (U_{Dn} - U_{an})^{-1/2} \right] \tag{10}$$

for multi-step tunneling and

$$J_Z \propto U_{an} \exp \left[\frac{-\alpha (E_{gn} - \Delta E_V)(U_{Dn} - U_{an})^{-1/2}}{R-1/2} \right] \tag{11}$$

for direct tunneling. E_{gn} is the energy gap of the n-material, and E_r is the tunneling barrier for each tunneling step (via n-region traps). When plotted on log-log scale, J_Z appears to be a power law function $J_Z \propto V_{an}^m$ where $m > 3$ for $|-V_{an}| > V_{Dn}$ and $m = 1$ for $|-V_{an}| < V_{Dn}$.

4.3 I-U Characteristics, Experimental

The forward I-U characteristics presented in Figs. 4 and 5 do not show exponential behavior and can not be directly linked to the functional dependence of J_e, J_r, J_s or J_n. These I-U characteristics are more indicative of space-charge-limited currents in the bulk ZnS, ZnSe when a substantial trap, distribution is present. The high power law region represents the filling of these traps while the break into a lower power law region represents the traps filled condition. Rose [34] has shown that for an exponential energy distribution of traps, $N_t \propto \exp (E/E_o)$, the injected space charge current is

$$J_{SCL} = \text{const } U_{an} \left(\frac{Eo}{kT} + 1\right) \qquad (12)$$

in the trap filling region. E is the trap energy, and E_o is a constant. When the injected space-charge is sufficient to occupy all the trap levels in the energy gap, the current becomes

$$J_{SCL} = \text{const } U_{an}^2 \qquad (13)$$

Both constants are mildly temperature dependent. Egn (12) indicates that the slope $\Delta \log J_{SCL}/\Delta U_{an}$ should be temperature dependent, and depend on the value of E_o. However the high power-law slopes seen in Fig. 4 are rather independent of temperature which suggest that if an exponential distribution of traps is the correct model, then E_o varies with temperature. One must be cautious in assuming that (12) is the correct functional dependence since more complicated trap distributions could lead to similar I-U characteristics.

The forward I-U results suggest that the true heterojunction I-U characteristic is masked by the space-charge-current flow in the moderately high resistivity ZnS, ZnSe. Similar space-charge effects have been seen in ZnSe-Ge [32] and ZnSe-GaAs [6] devices where the ZnSe resistivity was 10^3 ohm-cm. However, both the ZnSe-Ge [5] and ZnSe-GaAs [6] devices have shown transistor action (using the ZnSe as a wide-gap emitter) indicating that the injected interface current component J_n is substantial. Plans are under way to perform similar transistor experiments with the nZnS-pGaP pair.

A roughly ohmic region is observed at low voltages in the nZnS-pGaP forward I-U characteristic Fig. 4, that corresponds to either surface leakage or to the heterojunction characteristic. At low forward voltages the heterojunction impedance may be expected to be quite large since the diffusion voltage, U_D, is quite large. The resistance associated with the ohmic region is too large to be associated with the 5×10^3 ohm-cm ZnS. Similar ohmic regions were seen in both ZnSe-Ge [32] and ZnSe-GaAs [35] devices.

The power-law variation of reverse current with applied reverse voltage shown in Fig. 6 for an nZnS-pGaP diode suggests a tunneling mechanism of the form

$$I \propto U_a \exp\left[-M(U_a + U_D)^{-1/2}\right] \tag{14}$$

where M is given theoretically from (10) and (11) as

$$M = \alpha E_r^{1/2} R^{1/2} (E_{gn} - \Delta E_v) \tag{15}$$

for multi-step tunneling, and as

$$M = \alpha R^{1/2} (E_{gn} - \Delta E_v)^{3/2} \tag{16}$$

for direct tunneling.

M may be determined experimentally by replotting the data of Fig. 6 as log I/U_a versus log $(U_D+U_a)^{-1/2}$. This is shown in Fig. 9. The values of M are 30 at 300°K and 33 at 77°K. A value of U_D = 2 volts (obtained from capacitance data, Fig. 7) was used in Fig. 9. Using the values m^*/m^o = 0.19, $\varepsilon_n/\varepsilon_o$ = 8.3, $N_D = 1\text{x}10^{13}\text{cm}^{-3}$, $(E_{gn}-\Delta E_v)$ = 2.65 at 300°K and $(E_{gn}-\Delta E_v)$ = 2.68 at 77°K the theoretical values of M are $2.5\text{x}10^3\ E_r^{1/2}$ volts$^{1/2}$ at 300°K and $2.8\text{x}10^3\ E_r^{1/2}$ volts$^{1/2}$ at 77°K for the indirect tunneling process. A direct tunneling process must be ruled out by the large ZnS depletion width (about 1.8μm at zero bias).

To obtain agreement between experimental and theoretical slopes a value of $E_r \simeq 10^{-4}$ eV is necessary. This is an improbable value since it would correspond to

$$\frac{E_{gn}-\Delta E_v}{E_r} \simeq 2.65 \times 10^4$$

tunneling steps at 300°K. A very large number of band gap states would be required to support such small energy transitions. Since such a high density of band gap states is highly unlikely, a reverse transport mechanism other than a simple multi-step Zener tunneling process is operative in these n-ZnS-pGaP diodes even though the reverse I-U characteristic appears to agree qualitatively with that of a tunneling process. In fact we can not exclude a surface leakage mechanism since guard ring structures were not provided

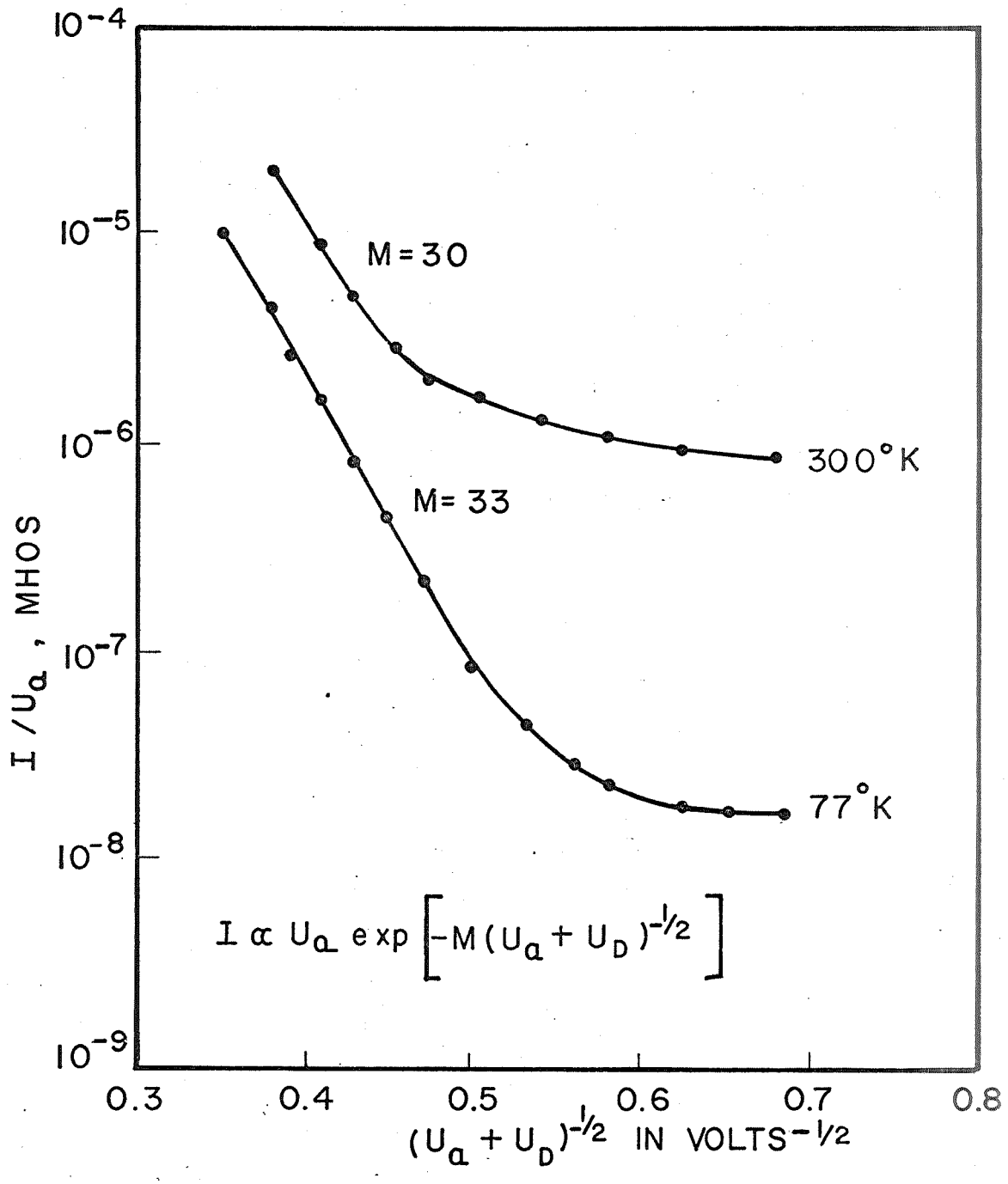

Fig. 9. Reverse bias U-I characteristic of Fig. 6 plotted in terms of I/U_a versus $(U_a + U_D)^{-1/2}$ to reveal functional dependence. U_D was taken as 2 volts.

because of fabrication problems.

The reverse current in nZnS-pGap diodes was orders of magnitude larger than that reported for ZnSe-Ge [32] and ZnSe-GaAs [35] diodes with 10^3 ohm-cm ZnSe resistivity that were fabricated in the same HCl growth system. Yet from band diagram considerations one would not expect the reverse current to be appreciably different between the two types of diodes. Both ZnS and ZnSe have wide depletion widths which should in part control tunneling current magnitudes. Avalanche multiplication occurs above 25 volts applied reverse voltage for both diode types (even including the large built-in field in the ZnS-GaP diodes) and should not affect current magnitudes below this voltage.

The larger-than-expected reverse current obtained with nZnS-pGaP devices is probably related to the source of the noise and jitter. It is tentatively suggested that the quality of the interface is responsible for the noise and jitter. The lattice mismatch is 1% which is about 4 times that of ZnSe-GaAs. Sufficient interfacial strain may have introduced dislocations into the ZnS layer which serve as extra trapping centers to promote reverse tunneling currents. Also nZnSe-pGaP devices (where the lattice mismatch is about 4%) exhibited more noise and jitter than did nZnS-pGaP devices, lending some support to the suggestion that noise and jitter are related to the interfacial strain. However, the GaP crystal quality (number of defects) and surface preparation (perhaps a thin insulating film remains on GaP after polishing) are also subject to question as sources of noise.

Robinson and Kun [13], who grew GaP on 0.1 ohm-cm ZnSe and 0.5 ohm-cm $ZnS_{0.45}Se_{0.55}$ by solution growth techniques, report noise-free V-I characteristics and reverse breakdown voltages greater than 15 volts in their devices. This indicates that (nZnSe, nZnS)-pGaP junctions with favorable characteristics can be successfully fabricated by solution techniques (although there is always a chance that a solid solution of ZnSe and GaP may be formed at the interface).

It remains to be shown whether the same degree of success can be achieved with the HCl vapor transport system by the use of better quality GaP substrate material in the future.

The Anderson band model (Fig. 8(a)) predicts a value of U_D = 2.2 volts for nZnS-pGaP doped to n ≃ 10^{13} cm^{-3} (ZnS) and p ≃ 5 x 10^{17} (GaP). This agrees fairly well with the values of U_D obtained from capacitance data (Fig. 7). The dependence of C and U_D on frequency can be attributed to the time response of levels in the moderately high resistivity ZnS. Such frequency effects have been observed in nZnSe-Ge [32] and nZnSe-GaAs diodes [5]. The slope r = 0.4 indicates that the ionized impurity profile at 1MHz and 1KHz may lie somewhere between that of a constant and a linear function of distance.

The absence of light emission in these devices is not understood. One might argue that defect currents due to interface states and interface strain dominate the forward conduction process resulting in no electron injection into the GaP. Or the recombination of injected electrons in the GaP may be non-radiative. Robinson and Kun [11] have observed light emission in nZnSe-pGaP diodes.

III. Ge-GeAs HETEROJUNCTIONS

1. Low Temperature Growth of Ge on GaAs by Iodine Transport

Work this quarter was directed toward the elimination of the unwanted homojunction at the emitter-base junction of the n-GaAs-p-Ge-n-Ge heterojunction transistor. As reported previously, the initial layer of germanium grown on high resistivity and n-type GaAs seeds has always been n-type, even when a p-type dopant has been present and the grown layers appeared p-type away from the interface. At first surface contamination due to seed preparation was suspected; however, inspection of the interface of p-doped layers grown on cleaved GaAs seeds by a previously reported thermal probe technique also showed an n-type layer. Next, a dopant delay due to redeposition of the dopant from the vapor phase onto the connecting tubing walls was hypothesized. A run in which a lengthy pre-flow through the dopant source was employed resulted in poor adhesion of the deposited layers due to an initial layer of boron deposited on the seeds. A heater wrap around the connecting tubing to keep the BI_3 in the vapor phase was only partially successful in that it did keep visible deposits from forming, but the interface remained n-type.

The transient nature of the initiation of growth was suspected to cause an initial rapid deposition of germanium as a surge of iodine from the previously sealed iodine column was admitted to the growth tube. This rapid growth of naturally occurring slightly n-type germanium was thought to overcome the p-type dopant present until a steady state flow was established. Attempts to pass this initial flow through the growth tube with the seeds at elevated temperature (600°C), thus preventing deposition until a steady state flow was established and the seed temperature lowered to 375°C for growth, were not totally successful. A skin of high resistivity material was found on all surfaces of the GaAs seeds before deposition started, probably from indiffusion of germanium, thus creating an additional unwanted layer in the device. In addition,

the germanium at the interface was still slightly n-type, although gentle pressure on the thermal probe would cause the reading to change toward p-type, indicating only a thin n-layer remained.

To provide for a dumping of the initial flow of iodine (actually hydrogen-iodide from the source catalytic converter), a bypass was constructed around the growth tube and out through the exhaust bubblers with suitable valves to control flows and isolate the various sections of tubing. While this portion of the system was disassembled, the intrinsic germanium source was removed and replaced with a larger, more fully packed source. Following a purging run to bring the surface of the new source germanium to growth cleanliness, a run was made in which the bypass was used to shunt the first few minutes of the iodine flow around the growth tube with the BI_3 connecting tube heater employed as well. A preflow of BI_3 was used which was kept below that which previously caused non-adhering layers. However, even this duration proved too long with the result that these layers adhered but had a matte appearance and showed a tendency to flake near the edges. The run was repeated with a very short BI_3 preflow but otherwise identical conditions. This growth was the usual shiny well adhering epi-layer and did indeed probe p-type at the interface. When mesa devices were made from a p-Ge seed which was present in the deposition region, a barrier of a few tenths of a volt was found between the grown layer and the seed from its I-V characteristic. The polarity of this characteristic and size of the barrier were such that the layer must have been near intrinsic p-type or slightly n-type in the interfacial layer even though the bulk of the grown material was 3×10^{-2} ohm cm p-type.

To eliminate again the possibility of some surface contaminant causing the interfacial layer, cleaved seeds were used. Since the total area presented for interface and device investigation in the previous cleaving of GaAs was extremely

small, it was desired to cleave a large area p-Ge sample for insertion into the growth tube. The procedure of Palmer et al.[36] for cleaving germanium was followed with a slight modification. The thick accurately oriented (111) sample was slotted along its top only, the bottom being rigidly held by a flat support. A wedge was then driven into the top slot causing the sample to cleave along the (111) plane starting at the slot edge and presenting flat stepless areas suitably large for subsequent mesa device fabrication. The bottom notch was eliminated when it was found that it did not improve either the ease or quality of the cleave.

A run was made using cleaved as well as conventional chemically polished seeds in which the growth tube bypass was employed, the BI_3 connecting tube heater used, but with no BI_3 preflow. The interface of this growth was only slightly n-type which went to p-type as pressure on the probe was increased indicating that the layer is very thin. Mesa devices made from the cleaved p-Ge seed showed a barrier (as expected from the interface layer) with an I-V characteristic similar to emitter-collector punch through of a low voltage transistor, albeit with a large leakage component.

The previous run was repeated including cleaved as well as chemically polished seeds, with the addition of a slight BI_3 preflow and an increase in dopant carrier flow during the run. The connecting tubing for the BI_3 was heated and a lengthy preflow through the tubing via an external bubbler was used. The interface layer on this growth probed just barely p-type. Devices fabricated from the cleaved p-Ge seeds, however, showed the presence of an interfacial layer.

At this time a supply of diborane in helium carrier became available. After a modification of the dopant introduction tip and coupling to permit the introduction of dopants directly into the deposition region without passing them through a higher temperature region (425°C vs 375-400°C in the deposition region),

a pair of runs was made using the new dopant supply. In the first run the layers grown were n-type throughout due to either the seeds having been placed too far downstream, the dopant flow being too low, or a combination of these. A distribution of seeds were placed in the next run, again with cleaved and chemically polished seeds present, and the amount of diborane increased. Probing of the interface from several of the seeds showed a p-type interface in those seeds which were closest to the point of dopant introduction and grading through a mixed p and n-type interface to a totally n-type interface in those which were furthest (5 cm) from the dopant inlet. Mesa devices made from the cleaved p-Ge seed closest to the dopant inlet showed an ohmic characteristic for currents up to 50 ma indicating no interfacial layer being present. Devices from identical cleaved p-Ge seeds which were further away showed a barrier as seen previously.

A possible explanation for this grading in doping is an initial depletion of the small amount of hydrogen iodide available in the deposition region. Elemental boron is thought to be liberated from the diborane through an intermediate reaction with the HI present to form BI_3 which then decomposes.[37] Diborane is not known to decompose directly to elemental boron and hydrogen at the temperatures involved.[38] A run is now being made to fabricate a transistor structure using the diborane as a dopant source and seeds placed in close proximity to the inlet to insure a uniform p-type layer at the interface.

2. Electrical Characteristics of a nGe-nGaAs Heterojunction

Further measurements were made on the n-Ge-n-GaAs heterojunction reported during the last period. The barrier height determined by extrapolating the $1/C^2$ versus voltage data to the infinite capacitance intercept was found to be .43 eV. Both forward and reverse I-V data were taken at a number of temperatures between room and liquid nitrogen as shown in Figure 10. The η values correspond to

the straight line portions of the respective curves. Using the analysis of Fang and Howard,[39] the zero voltage intercept of the linear portion of the reverse I-V data is plotted as a function of 1/T as shown in Figure 11. The barrier height deduced by a least squares fit to the slope of this line for our junction on the (111)As face is .37 eV in agreement with the same value arrived at by Fang and Howard for their devices. This should correspond to the ΔE_c value for Ge-GaAs but is considerably greater than the value of $\sim$ 0.15 obtained from measurements on n-p and p-n Ge-GaAs junctions. We plan to look at a variety of n-n, p-p, n-p and p-n junctions with this growth system to help clarify this apparent inconsistency.

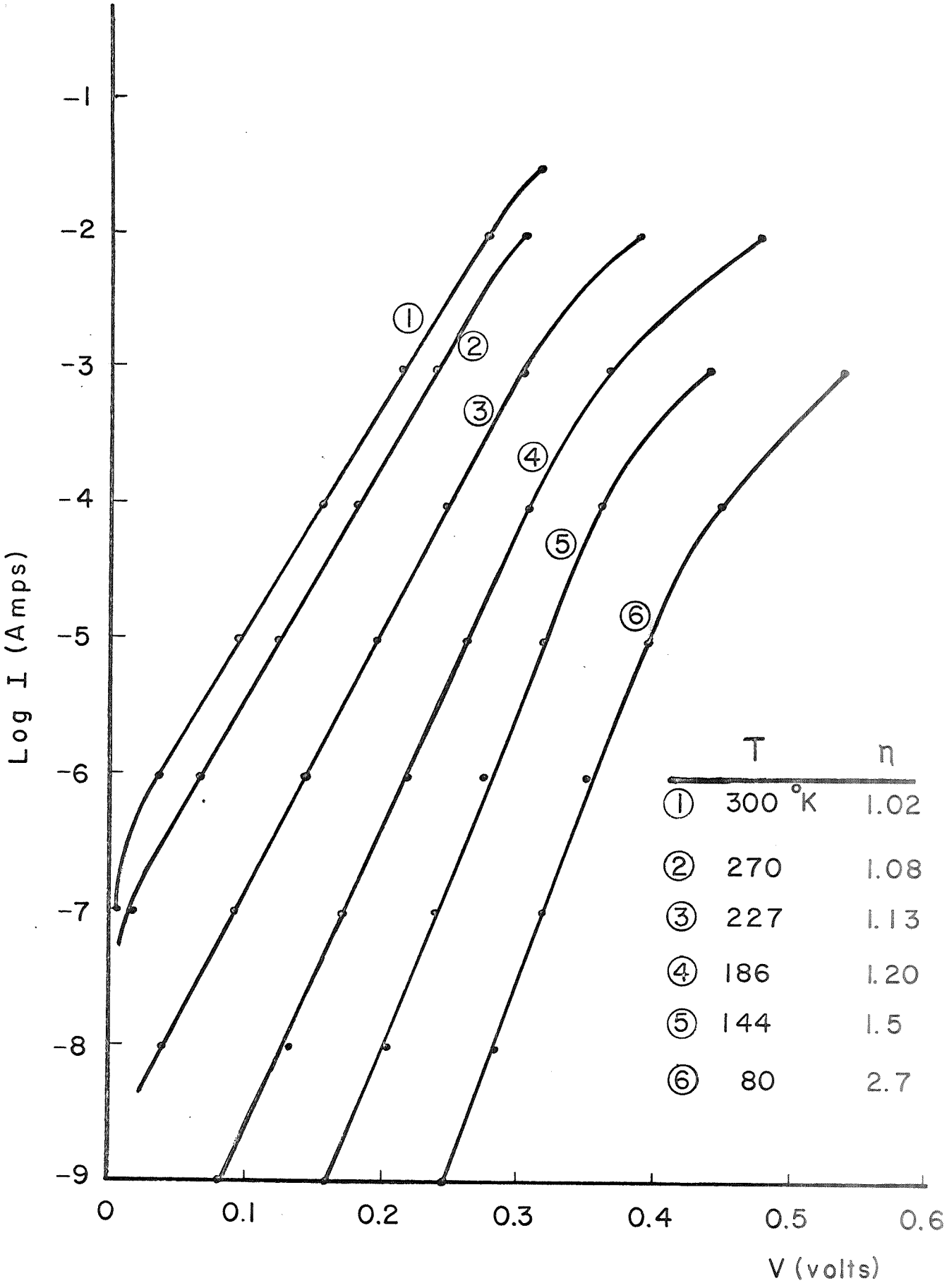

Fig. 10 Forward current-voltage characteristic of n-Ge ($10^{16}/cm^3$) - nGaAs ($5 \times 10^{15}/cm^3$) heterojunction.

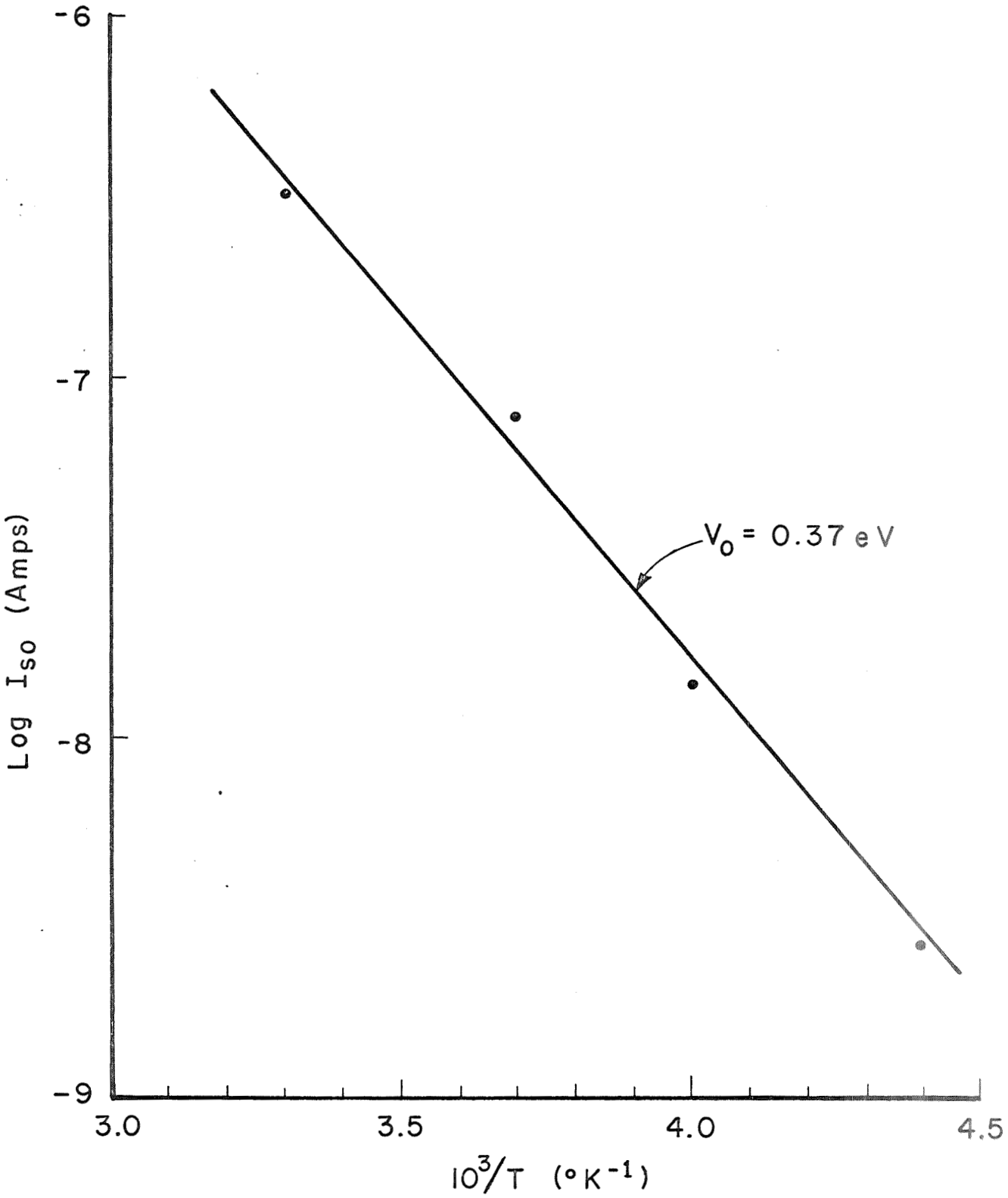

Fig. 11 Zero voltage intercept of reverse saturation current vs reciprocal temperature for nGe - nGaAs heterojunction

IV. REFERENCES

[1] H. Kroemer, Proc. IRE 45, 1535 (1957).

[2] S. Brojdo, T. Riley and G. T. Wright, Brit. J. Appl. Phys. 16, 133 (1965).

[3] R. Zuleeg and P. Knoll, Final Report, Hughes Aircraft Co., N66-37312, available National Technical Information Service, Springfield, Va. USA.

[4] D. K. Jadus and D. L. Feucht, IEEE Trans. Electron Dev. ED-16, 102 (1969).

[5] H. J. Hovel and A. G. Milnes, IEEE Trans. Electron Dev. ED-16, 766 (1969).

[6] K. J. Sleger, A. G. Milnes and D. L. Feucht, Proc. Int. Conf. Phys. Chem. of Semiconductor Heterojunctions and Layer Structures, Hungarian Academy of Sciences, Budapest, October, 1970.

[7] M. B. Panish and I. Hayashi, Proc. Int. Conf. Phys. Chem. of Semiconductor Heterojunctions and Layer Structures, Hungarian Academy of Sciences, Budapest, October, 1970.

[8] Zh. I. Alferov, V. M. Andreev, E. L. Portnoi, and M. K. Trukan, Sov. Phys. Semiconductors 3, 1107 (1970).

[9] G. A. Zholkevich, Optics and Spectroscopy 18, 500 (1965).

[10] M. V. Kot, L. M. Panasyuk, A. V. Simashkevich, A. E. Tsurkan and D. A. Sherban, Sov. Phys. Solid State 7, 1001 (1965).

[11] Y. Tsujimoto and M. Fukai, Jap. J. Appl. Phys. 6, 1024 (1967).

[12] Zh. I. Alferov, D. Z. Garbuzov, V. S. Grigor'eva, Yu. V. Zhulyaev, L. V. Kradinova, V. E. Korol'kov, E. P. Morozov, O. A. Ninna, E. L. Portnoi, V. D. Prochukhan and M. K. Trukan, Sov. Phys. Solid State 9, 208 (1967).

[13] R. J. Robinson and Z. K. Kun, Appl. Phys. Lett. 15, 371 (1969).

[14] A. V. Vanyukov, A. N. Kovalev, N. M. Kondaurov, V. A. Supalov and Yu. A. Fedotov, Sov. Phys. Semiconductor 4, 1157 (1971).

[15] I. Bertoti, M. Farkas-Jahnke, E. Lendvay and T. Nemeth, J. Mat. Sci. 4, 699 (1969).

[16] J. S. Hill, T. G. R. Rawlins and G. N. Simpson, Report No. 69049 Signals Research and Development Establishment, AD707343, available National Technical Information Service, Springfield, Va., USA.

[17] H. J. Hovel and A. G. Milnes, J. Electrochem. Soc. 116, 843, (1969).

[18] G. W. Heunisch, J. Electrochem. Soc. 114, 642 (1967).

[19] M. Aven, U.S. Patent #3,146,204 (1964).

[20] D. K. Jadus, H. E. Reedy and D. L. Feucht, J. Electrochem. Soc. 114, 408 (1967).

[21] H. C. Casey, Jr., and F. A. Trumbore, Mat. Sci. Eng. 6, 69 (1970).

[22] E. G. Dierschke and G. L. Pearson, J. Appl. Phys. 41, 329 (1970).

[23] I. Bertoti, M. Farkas-Jahnke, M. Harsy, T. Nemeth and K. Richter, Proc. Int. Conf. on Luminescence, Hungarian Academy of Sciences, Budapest, 1261 (1966).

[24] W. L. Roth, Acta. Cryst. 13, 1064 (1960).

[25] R. L. Anderson, Solid State Elect. 5, 341 (1962).

[26] R. K. Swank, Phys. Rev. 153, 844 (1967).

[27] M. Weinstein, R. O. Bell and A. A. Menna, J. Electrochem. Soc. 111, 674 (1964).

[28] Zh. I. Alferov, V. I. Korol'kov and M. K. Trukan, Sov. Phys. Solid State 8, 2813 (1967).

[29] M. Cowley and H. Heffner, J. Appl. Phys. 35, 255 (1964).

[30] G. W. Gobeli and F. G. Allen, Phys. Rev. 137, A245 (1965).

[31] M. E. Davis, G. Zeidenbergs and R. L. Anderson, Phys. Stat. Sol. 34, 385 (1969).

[32] H. J. Hovel and A. G. Milnes, Int. J. Electronics 25, 201 (1968).

[33] A. R. Riben and D. L. Feucht, Int. J. Electronics 20, 583 (1966).

[34] A. Rose, Phys. Rev. 97, 1538 (1955).

[35] K. J. Sleger, Ph.D. Thesis, Carnegie-Mellon University, available from University Microfilms, Ann Arbor, Mich., USA.

[36] D. R. Palmer, S. R. Morrison and C. E. Davenbaugh, J. Phys. Chem. Solids, 14, 27 (1960).

[37] M. Berkenblit and A. Reisman, J. Electrochem. Soc., 117, 1100 (1970).

[38] G. G. Devyatykh and A. S. Yushub, Russian Journal of Physical Chemistry, 38, 957 (1964).

[39] F. F. Fang and W. R. Howard, J. Appl. Phys., 35, 612 (1964).

V. PUBLICATIONS

During this report period the following two papers appeared in Volume I of the Proceedings of the International Conference on the Physics and Chemistry of Semiconductor Heterojunctions and Layer Structures.

"Preparation and Properties of Ge-Ge_xSi_{1-x}, Ge-GaAs and Si-GaP Heterojunctions," D. L. Feucht, I, I-39 - I-62, Akademiai Kiado, Budapest 1971.

"ZnSe-GaAs and ZnSe-Ge Heterojunction Transistors," K. J. Sleger, A. G. Milnes and D. L. Feucht, I, I-73 - I-92, Akademiai Kiado, Budapest 1971.

VI. CONTRIBUTORS

Dr. D. L. Feucht, Professor of Electrical Engineering

Dr. A. G. Milnes, Professor of Electrical Engineering

D. Howarth, Graduate Student, Ph.D. level

K. Sleger, Graduate Student, Ph.D. level